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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,589	08/24/2001	Mahito Shinohara	35.C15697	3628
5514	7590	09/09/2004	EXAMINER	
FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112			MISLEH, JUSTIN P	
			ART UNIT	PAPER NUMBER
			2612	6

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/935,589

Applicant(s)

SHINOHARA, MAHITO

Examiner

Justin P Misleh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/24/01 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5</u> . | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 18 (page 4, line 10).
3. Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim 5** recites the limitation “wherein the read transistor amplifies and outputs a signal in the control electrode area from one of the main electrode areas, and wherein said signal line is connected to an other main electrode area of the read transistor”. There is insufficient antecedent basis for this limitation in the claim.

Turning to parent Claim 2, which requires: “a read transistor for reading a signal from the photoelectric conversion unit and a reset transistor for resetting an input portion of the read transistor, wherein the reset transistor is turned on/off by controlling a control electrode area thereof, and a signal line for supplying a predetermined signal level to operate the read transistor, wherein the signal line is connected to one of main electrode areas of said reset transistor”.

Claim 5 does not introduce or define a “control electrode area” or “one of main electrode areas” of the read transistor so it cannot refer back to them. The failure to provide explicit antecedent basis for these terms renders the claim indefinite. The scope of Claim 5 is not reasonably ascertainable by those skilled in the art. See MPEP 2173.05(e) [R-1].

The Examiner recommends that Claim 5 introduce individual components of the read transistor and identify the difference between the individual components of the read transistor and the individual components of the reset transistor (as defined in Claim 2), and then proceed to list any limitations concerning the supply line. For the purposes of examination, the Examiner will interpret Claim 5 as the above identified recited limitation of Claim 2; thus, the rejection of Claim 2 fully encompasses the newly interpreted limitations of Claim 5.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1 – 11** are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al.

8. For **Claim 1**, Kim et al. disclose, as shown in figures 1, 4, and 5 and as stated in columns 4 (lines 60 – 67) and 5 (lines 1 – 24), a solid-state image pickup apparatus (400) comprising:

a pixel (400) including a photoelectric conversion unit (401 and 402), a read transistor (M3) for reading a signal from said photoelectric conversion unit (401 and 402), and a reset transistor (M1) for resetting an input portion of said read transistor (M3; When the reset transistor M1 is turned on, vdd flows through the reset transistor M1 and onto the gate of the read transistor M3, thereby also turning on the read transistor M3, wherein vdd also flows through an source input portion of the read transistor M3); and

an output line (data-out) to which the signal from the read transistor (M3) is read out (by means of selecting transistor M4), wherein the reset transistor (M1) is controlled in accordance with a signal level of said output line (data-out; see explanation below).

Kim et al. disclose the operation of the pixel (400) in figure 5. As shown in figure 5, the reset transistor M1 is turned on (by means of Rx) after a time period F1 and after a time period F2, wherein time periods F1 and F2 each represent a pixel signal output period. Therefore, the reset transistor M1 is only turned on (hence in conformity) after a pixel signal output period to

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clear the output line (from the pixel signal output) wherein the output line becomes ready to output another pixel signal. The pixel signal output will always have some signal level; therefore, the reset transistor M1 is controlled in accordance with a signal level of the output line (data-out). In other words, the reset transistor M1 is only turned on upon the output of a pixel signal (with some signal level) onto the output line (data-out).

9. For **Claims 2 and 5** (please see the 112, 2<sup>nd</sup> paragraph rejection of Claim 5 above), Kim et al. disclose, as shown in figures 1, 4, and 5 and as stated in columns 4 (lines 60 – 67) and 5 (lines 1 – 24), a solid-state image pickup apparatus (400) comprising:

a plurality of pixels (Pixel Array 20 as in figure 1) arrayed in horizontal (N) and vertical directions (M; also see column 1, line 55 – 59), each pixel including a photoelectric conversion unit (401 and 402), a read transistor (M3) for reading a signal from the photoelectric conversion unit, and a reset transistor (M1) for resetting an input portion of the read transistor, wherein the reset transistor is turned on/off by controlling a control electrode area thereof (The gate of M1 is a control electrode area of M1; wherein the gate of M1 is controlled by control signal Rx.); and

a signal line (vdd) for supplying a predetermined signal level to operate the read transistor, wherein the signal line (vdd) is connected to one of main electrode areas (The source of M1 is a main electrode area of M1; wherein the source of M1 is connected to vdd.) of said reset transistor (M1), and the signal line (vdd) independently supplies a signal on a unit basis of said plurality of pixels in a horizontal direction (see explanation below).

The Examiner believes the “signal line independently supplies a signal on a unit basis of said plurality of pixels in a horizontal direction” limitation corresponds to figure 2 of Applicant’s figures and pages 14 (lines 26 and 27) and 15 (lines 1 – 6) of Applicant’s specification, because

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Applicant states that the power supply line 46 is applicable to selected pixels. Kim et al. provides each pixel with a selecting transistor M4 for selecting each pixel on a unit basis independently by means of select signal (Sx) provided by (control electronics as shown in figure 1), thus satisfying the cited limitation.

10. As for **Claim 3**, Kim et al. disclose, as shown in figure 4, a control transistor (select transistor M4) connected to said output line (data-out) to control the signal level of said output line (select transistor M4 turns the control line on or off).

11. As for **Claim 4**, Kim et al. disclose, as shown in figures 4 and 5, an output line (data-out) arranged on the unit basis of said plurality of pixels in the horizontal direction (the unit basis feature is described above in regards to Claim 2), to which a signal from the read transistor (M3) is read out (by means of select transistor M4), wherein the reset transistor is controlled in accordance with a signal level of said output line (see explanation below).

Kim et al. disclose the operation of the pixel (400) in figure 5. As shown in figure 5, the reset transistor M1 is turned on (by means of Rx) after a time period F1 and after a time period F2, wherein time periods F1 and F2 each represent a pixel signal output period. Therefore, the reset transistor M1 is only turned on (hence in conformity) after a pixel signal output period to clear the output line (from the pixel signal output) wherein the output line becomes ready to output another pixel signal. The pixel signal output will always have some signal level; therefore, the reset transistor M1 is controlled in accordance with a signal level of the output line (data-out). In other words, the reset transistor M1 is only turned on upon the output of a pixel signal (with some signal level) onto the output line (data-out).

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12. As for **Claims 6 and 7**, Kim et al. disclose, as stated in column 2 (lines 64 – 67), wherein the read transistor and reset transistor are MOS transistors.

13. As for **Claims 8 and 9**, Kim et al. disclose, as shown in figures 4 and 5, a transfer switch (M43) between the photoelectric conversion unit (401) and the read transistor (M3), wherein signal charges accumulated in the photoelectric conversion unit are transferred to the input portion of the read transistor through said transfer switch (At time period F1).

14. As for **Claims 10 and 11**, Kim et al. disclose, as shown in figures 4 and 5, wherein a plurality of transfer switches (M43 and M44) are connected to the input portion of the read transistor (The transfer switches M43 and M44 are connected to the gate of read transistor M3 and to the source of read transistor M3, by means of reset transistor M1), and signal charges are independently transferred from a plurality of photoelectric conversion units by said transfer switches (In independent time periods F1 and F2; see figure 5).

### ***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. **Claims 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al.

17. As for **Claims 12 and 13**, Kim et al. do not disclose an image pickup system comprising said solid-state image pickup apparatus; an optical system adapted to form an image of light onto



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said solid-state image pickup apparatus; and a signal processing circuit adapted to process an output signal from said solid-state image pickup apparatus. **Official Notice** is taken that both the concepts and the advantages of providing an image pickup system comprised of an optical system and a signal processing circuit are well known and expected in the art. It would have been obvious to one with ordinary skill in the art to have provided an image pickup system comprised of an optical system and a signal processing circuit as a means to generate a focused, high resolution, low noise digital image.

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Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM

September 4, 2004



NGOC-YEN VU  
PRIMARY EXAMINER